Customer No.: 31561
Docket No.: 10296-US-PA
Application No.: 10/605,161

In The Claims:

Claim 1. (currently amended) A method of coupling a host that is equipped with a central processing unit (CPU) level processing capacity, a non-volatile random access memory (NVRAM), and at least a controller together to allow the host to access the NVRAM and the controller, the method comprising:

~~OLE_LINK1~~ transmitting an instruction and a pragmatic bit from the host to the controller and the NVRAM, wherein the controller is coupled with the host and the NVRAM, respectively via a chip-select line, a system-clock line and a data transmission_wiring ~~OLE_LINK1~~;

indicating the instruction either for the NVRAM or for the controller by the pragmatic bit which is accompanied with the instruction;

turning either the NVRAM or the controller on/off according to the pragmatic bit; and

executing the instruction either at the NVRAM or at the controller to control simultaneously the NVRAM and the controller.

Claim 2. (currently amended) The method of claim 1, wherein the data transmission wiring_comprises a data-input line to construct a 3-wire mechanism for transmitting the instruction and the pragmatic bit.

Claim 3. (currently amended) The method of claim 1, wherein the data transmission wiring_comprises a data-input line and a data-output line to construct a 4-wire mechanism for transmitting the instruction and the pragmatic bit.

Claim 4. (currently amended) The method of claim 1, wherein the pragmatic bit is a binary bit appended to the end of the instruction that is issued from the host to the NVRAM and the controller.

Claim 5. (original) The method of claim 4, wherein the binary bit respectively triggers the NVRAM and the controller to respond to the instruction when it is respectively at two different states.

Claim 6. (original) The method of claim 1, wherein the instruction disables signal transmissions of the NVRAM responsive to the data transmission wiring and the system-clock line if the instruction is for the controller according to the pragmatic bit.

Claim 7. (original) The method of claim 1, wherein the instruction enables signal transmissions of the NVRAM responsive to the data-input line and the system-clock line if the instruction is for the NVRAM according to the pragmatic bit, and the signal transmissions of the controller responsive to the data-input line and the system-clock line are disabled.

Claim 8. (original) The method of claim 1, further comprising a step of appending setup information to the pragmatic bit to set the controller according to the setup information if the instruction is used to configure the controller before the step of transmitting the instruction and the pragmatic bit.

Claim 9. (original) The method of claim 1, wherein the controller transmits data to the host after the controller receives the pragmatic bit if the host issues the instruction to read the data from the controller during the step of executing the instruction.

Claim 10. (currently amended) A multi-access architecture of a non-volatile memory, comprising:

a host for transmitting an instruction and a pragmatic bit via a first chip-select line, a system-clock line and a data transmission wiring, wherein the pragmatic bit is accompanied with the instruction;

a non-volatile random access memory (NVRAM) electrically connected to the host by the system-clock line and the_data transmission_wiring so that the host is able to access the NVRAM; and

at least a controller electrically connected to the host and the NVRAM via the first chip-select line, a second chip-select line, the system-clock line and the_data transmission wiring, respectively for differentiating the instruction sent to the NVRAM from the instruction sent to the controller according to the pragmatic bit, wherein the instruction is executed either at the NVRAM or at the controller to control simultaneously the NVRAM and the controller so that the pragmatic bit turns on/off the NVRAM and the controller.

Claim 11. (currently amended) The multi-access architecture of claim 10, wherein the data transmission wiring_comprises a data-input line to construct a 3-wire mechanism for transmitting the instruction and the pragmatic bit.

Claim 12. (currently amended) The multi-access architecture of claim 10, where-in the data transmission wiring_comprises a data-input line and a data-output line to construct a 4-wire mechanism for transmitting the instruction and the pragmatic bit.

Claim 13. (currently amended) The multi-access architecture of claim 10, wherein the pragmatic bit is a binary bit appended to the end of the instruction that is issued by the host to the NVRAM and the controller.

Claim 14. (original) The multi-access architecture of claim 13, wherein the binary bit respectively triggers the NVRAM and the controller to respond to the instruction when it is respectively at two different states.

Claim 15. (original) The multi-access architecture of claim 10, wherein the instruction disables signal transmissions of the NVRAM responsive to the data transmission wiring and the system-clock line if the instruction is for the controller according to the pragmatic bit.

Claim 16. (original) The multi-access architecture of claim 10, wherein the instruction enables signal transmissions of the NVRAM responsive to the data-input line and the system-clock line if the instruction is for the NVRAM according to the pragmatic bit, and the signal transmissions of the controller responsive to the data-input line and the system-clock line are disabled.

Claim 17. (original) The multi-access architecture of claim 10, wherein the pragmatic bit comprises setup information to set the controller if the instruction is for the controller.

Claim 18. (original) The multi-access architecture of claim 10, wherein the controller transmits data to the host if the host issues the instruction to read the data from the controller.

Claim 19. (original) The multi-access architecture of claim 10, further comprising a AND gate having a plurality of input terminals of the first chip-select

line and the second chip-select line and having an output terminal to be coupled with the NVRAM.